

REMARKS

Examiner's interview:

The Applicants had a telephone interview with Examiner Trujillo on August 3, 2004 to discuss the office action. The Applicants clarified that the Examiner meant that the Specification was objected to as lacking support for the terms "thermo-electric cooler" and "chilled fluid" and "solid state" cooling units. The Applicants pointed out where in the Specification "active cooling units" are found and indicated that a search for active cooling units on the Internet yielded thermo-electric coolers and solid state coolers. The Applicants included that web site in this response for the Examiner's review. The Examiner agreed that this would be acceptable. The Applicants discussed why "data defining a desired processor power consumption level" in Claim 15 is not redundant.

The Applicants explained to the Examiner how FIG. 1 is amended to include legends as suggested by the Examiner. The Applicants described how FIG. 2 is amended to include "first receiving circuit", "second receiving circuit", "third circuit", "fourth circuit", and "fifth circuit" as recited in Claim 19. The Applicants have included the excerpt from the Specification indicating support for labeling these elements. The Examiner agreed that this would be acceptable. The Applicants described how FIG. 3 is amended to include pictorials for the cooling fans and cooling units that are described in detail in the Specification. The Applicants have included the page number and line number where the Examiner can find the support for the amendment.

The Applicants discussed with the Examiner that the present invention recites a global view of power/performance management extending to delivery of customer level operational performance. The Examiner felt that amending the independent claims so that the first parameters corresponded to customer level operational requirements of the MP system may, pending further review by the Examiner, put this case in condition for

allowance. The Applicants have amended Claims 1, 19 and 24, accordingly, per the Examiner's suggestion.

Claims 1-33 are pending in the application.

New drawings FIG 1, FIG 2 and FIG 3 are included with changes suggested by the Examiner. FIG 1 has added legends to correspond to the Specification. FIG 2 has been amended to add circuitry to power/performance controller 201 described in the Specification. FIG 3 has been amended to add various cooling means with legends described in the Specification.

I. SPECIFICATION

The Examiner objected to the specification as failing to provide proper "antecedent basis for the claimed subject matter." The Applicants assume the Examiner meant "lack of support for the claimed subject." The Examiner specifically points out the "thermo-electric cooler in Claim 6 and "chilled fluid" and "solid state" cooling units in Claim 23. In the Specification of the present invention on page 13, lines 10-16 is the following:

"These actions include but are not limited to modifying the clock frequency and supply voltage of core logic in individual processor units on a multiprocessor VLSI chip, modifying the global frequency and supply voltage of I/O logic circuits, adjusting local cooling fan speed or active cooling devices on individual VLSI chips, adjusting cooling fans on system level processing units (e.g., servers), adjusting the cooling fans and air conditioning for multiple, stand-alone processing units (e.g., racks of servers) and suspending operation (various modes of sleep) of individual multiprocessor VLSI chips, stand-alone MP systems, or MP system clusters."

A search of the internet using "active cooling devices" resulted in this reference at www.shieldselectronics.com. "The Active Coolers available at SHIELDS Electronics Supply make use of a thermoelectric module to cool your CPU. A thermoelectric cooler (TEC) is a small solid state device that consists of a number of p and n- type pairs

connected electrically in a series and sandwiched between two ceramic plates. When connected to a DC power source, the Peltier effect causes heat to move from one side of the TEC to the other. This process creates a hot side and a cold side on the TEC. The cold side reduces CPU temperature dramatically, and the fan on the cooler serves only to draw the heat away from the TEC. These cooling units are designed to aid in overclocking, but are not recommended for processors over 1 Ghz. Please allow two weeks for delivery of these special items." It is well understood in the art that active cooling devices include thermoelectric coolers. It is also well known in the art that air conditioning systems cool by using "a chilled fluid" that results from compressing a gas, cooling the gas, and then expanding the gas or using evaporation methods to create a chilled fluid that is then used with a heat exchanger to remove heat from a surface or from an air stream feeding into a unit.

II. DRAWINGS

The Examiner objected to the drawings as failing to comply with 37 C.F.R. §1.83(a). The Applicants have amended FIGS. 1-3 as suggested by the Examiner.

The Examiner objected to the drawings as not showing elements claimed in Claim 19 of the present invention. Specifically, the Examiner objected to "first receiving circuit", "second receiving circuit", "third circuit", "fourth circuit", and "fifth circuit" in Claim 19. Claim 19 is directed to a controller for managing power and performance.

FIG 2 is a block diagram of power/performance controller 201. The description of power/performance controller 201 is found on page 15, line 7 through page 16, line 9. "FIG 2 is a block diagram of a power/performance controller 201 according to embodiments of the present invention. Controller 201 may be either a state machine or a programmed controller executing a set of software instructions. Controller 201 receives physical parameters (outputs of various temperature sensors) 207 or other physical parameters 206. [First and second receiving circuits] Other physical parameters 206 may include, but are not limited to, acoustic noise levels, vibration levels, EMC noise levels, etc. Controller 201 also receives quality of service parameters 205. Quality of

service parameters 205 may be parameters identifying guaranteed customer accessibility to processors, guaranteed bandwidth of processing, etc. Policy parameters 204 are values that define the cost of power, the availability of power, acceptable EMC levels, acoustic noise levels, etc. Logic or program instructions within controller 201 receive these parameters (204 through 207) and are configured to determine sets of global and local controls 202 and 203, respectively [**Third circuit**]. For example, all or a portion of parameter data 207 may include outputs 107 and 108 from multiprocessor VLSI chip 101. These controls are used to set the various processors (e.g., 103, 104, 105, and 106) at power and performance levels [**Fifth circuit**] by adjusting their supply voltages, clock frequencies, and cooling. The controls 202 and 203 may include signals that allow individual processors to be set to an operational or sleep mode. Embodiments of the present invention may implement controller 201 as with certain distributed functions. Controller 201 may issue some signals to set an MP system to a certain global power level [**Fourth circuit**] and additional control circuits in the MP system may determine how the power level is distributed between the individual processors in the MP system to achieve the global goal and global MP system performance goals. For example, set points 109 and 110 may include one or more of controls 202 and 203.

Additionally, the detailed descriptions of FIG. 3 and FIG. 4 describe in detail the various logic functions, receiving functions, control generating functions, etc. that power/performance controller 201 to give support for amending FIG. 2 to show the circuitry claimed in Claim 19 and described in the Specification.

The Examiner objected to the drawings for not illustrating "cooling means" as per Claims 4, 18, 21, 29, and 32, "cooling fan" as per Claims 5, 16, and 29, "thermo-electric" cooler" as per Claim 6, and "chilled fluid and solid state cooling units" as per Claim 23.

The Applicants have shown In The Specification above that there is support for the various cooling devices referred to in the claims. Also, the Applicants have shown that it is understood in the art that active cooling devices include thermo-electric coolers which are solid state cooling devices. Therefore, the Applicants have amended FIG. 3 to

illustrate with designators the various cooling means described in the Specification on page 13, lines 10-16. The following from page 13, lines 10-16 is repeated including designators to show how the drawings are amended to correspond to the Specification. Likewise, the designators used in the drawings are added to the Specification to make the Specification conform to the drawings. Relative to FIG. 3 is the following:

"These actions include but are not limited to modifying the clock frequency and supply voltage of core logic in individual processor units on a multiprocessor VLSI chip, modifying the global frequency and supply voltage of I/O logic circuits, adjusting local cooling fan speed (added cooling fan 322) or active cooling devices (thermo-electric cooler 323) on individual VLSI chips, adjusting cooling fans on system level processing units (e.g., servers)(cooling fan 321), adjusting the cooling fans and air conditioning for multiple, stand-alone processing units (e.g., racks of servers)(cooling system 324) and suspending operation (various modes of sleep) of individual multiprocessor VLSI chips, stand-alone MP systems, or MP system clusters."

On page 11, lines 15-16 of the Specification is the following: "The system rack may also have a central cooling unit in the form of ducted conditioned air or a separate rack fan."

The Examiner objected to FIG. 1 as lacking suitable descriptive legends to better understand the drawings. Even though the designated elements in FIG. 1 are described in detail in the Specification, the Applicants amended FIG. 1 to add legends to the VLSI chip 101, the core logic 113, 123, 133, and 143, processors 103-106, and I/O circuits 111, 114 and core logic circuits 112.

III. CLAIM OBJECTIONS

The Examiner objected to Claim 15 because the Examiner was of the opinion that "data defining a desired processor power consumption level" is redundant and should be deleted. Claim 15 is directed to the method of claim 1, wherein said power and performance goals comprise data defining a desired MP system power consumption level,

data defining a desired processor power consumption level, data defining desired MP system temperatures, desired MP acoustic noise output levels, desired EMC noise levels, and desired processor instruction execution speeds. The Applicants assert that the MP system power consumption level and the processor power consumption level are two different elements. The power consumption level for the MP system relates to the total power consumption of a sum of processor power consumptions, and processor power consumption relates to an individual processor. The Applicants assert that "data defining a desired processor power consumption level" is not redundant and the above argument traverses the objection of Claim 15.

IV. REJECTION UNDER 35 U.S.C. § 102

The Examiner rejected Claims 1, 19, 24 and 33 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,502,838 to *Kikinis* (hereafter "*Kikinis*").

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

The Applicants have amended Claims 1, 19, and 24 as suggested by the Examiner. The Examiner has stated with the amendments he believes Claims 1, 19, and 24 are differentiated from *Kikinis* and from the prior art pending a possible search by the Examiner. Therefore, the Applicants respectfully assert that the amendments to Claims 1, 19, and 24 traverse the rejections of these claims under 35 U.S.C. §102(e) as being anticipated by *Kikinis*.

Claim 33 is dependent from Claim 24 and contains all the limitations of Claim 24. Therefore, the Applicants respectfully assert that the rejection of Claim 33 under 35 U.S.C. §102(e) as being anticipated by *Kikinis* is traversed by the amendment to Claim 24.

Claims 11-12 are dependent from Claim 1 and contain all the limitations of Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claims 11-12 under 35 U.S.C. §102(e) as being anticipated by *Kikinis* are traversed by the amendment to Claim 1.

V. REJECTION UNDER 35 U.S.C. § 103

The Examiner rejected Claim 25 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of U.S. Patent No. 6,157,989 to *Collins et al.* (hereafter “*Collins*”). Claim 25 is dependent from Claim 24 and contains all the limitations of Claim 24. Therefore, the Applicants respectfully assert that the rejection of Claim 25 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Collins* is traversed by the amendment to Claim 24.

The Examiner rejected Claims 3 and 27 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Collins*. Claim 3 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 27 is dependent from Claim 24 and contains all the limitations of Claim 24. Therefore, the Applicants respectfully assert that the rejections of Claims 3 and 27 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Collins* are traversed by the amendment to Claims 1 and 24, respectively.

The Examiner rejected Claims 2, 15-18, 20-23, and 26 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of U.S. Patent No. 6,397,343 to *Williams et al.* (hereafter “*Williams*”). Claims 2 and 15-16 are dependent from amended Claim 1 and contain all the limitations of Claim 1. Claims 20-21 are dependent from Claim 19 and Claims 22-23 are dependent from Claim 21 and thus contain all the limitations of Claim 19. Claim 26 is dependent from Claim 24 and contains all the limitations of Claim 24. Therefore, the Applicants respectfully assert that the rejections of Claims 2, 15-18, 20-23, and 26 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Collins* are traversed by the amendment to Claims 1, 19, and 24.

The Examiner rejected Claims 4-6 and 28-29 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Collins* and further in view of *Williams*. Claims 4-6 are indirectly dependent from Claim 1 and contain all the limitations of Claim 1 and any intervening claims. Claims 28-29 are indirectly dependent from Claim 24 and contain all the limitations of Claim 24 and any intervening claims. Therefore the Applicants respectfully assert that the rejections of Claims 4-6 and 28-29 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Collins* and further in view of *Williams* are traversed by the amendments to Claims 1 and 24.

The Examiner rejected Claims 7-9 and 30-32 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Collins* and *Williams* further in view of the Applicants' prior art. Claims 7-9 are indirectly dependent from Claim 1 and contain all the limitations of Claim 1 and any intervening claims. Claims 30-32 are indirectly dependent from Claim 24 and contain all the limitations of Claim 24 and any intervening claims. Therefore the Applicants respectfully assert that the rejections of Claims 7-9 and 30-32 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Collins* and *Williams* further in view of the Applicants' prior art are traversed by the amendments to Claims 1 and 24.

The Examiner rejected Claims 10 and 14 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Williams*, U.S. Patent No. 6,639,883 to *Vladimir* (hereafter "*Vladimir*") and further in view of U.S. Patent No. 5,906,315 to *Lewis* (hereafter "*Lewis*"). Claims 10 and 14 are indirectly dependent from Claim 1 and contain all the limitations of Claim 1 and any intervening claims. Therefore, the Applicants respectfully assert that the rejections of Claims 10 and 14 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis* in view of *Williams*, *Vladimir* and further in view of *Lewis* are traversed by the amendments to Claim 1.

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

V. CONCLUSION

FIGS. 1-3 have been amended as suggested by the Examiner.

The Specification has been amended as to conform to the amended FIGS. 1-3.

Claims 1, 19, and 24 have been amended as suggested by the Examiner to differentiate the present invention from the prior art.

The Applicants have traversed the objection of Claim 15 as having redundant material.

The Applicants have traversed the rejections of Claims 1, 19, 24 and 33 under 35 U.S.C. §102(e) as being anticipated by *Kikinis*.

The Applicants have traversed the rejections of Claims 2-18, 20-23, and 25-32 under 35 U.S.C. §103(a) as being unpatentable over *Kikinis*, *Collins*, *Williams*, *Vladimir*, *Lewis*, and admitted prior art.

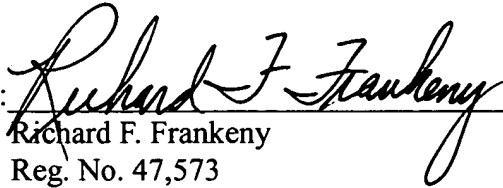
The Applicants, therefore, respectfully assert that Claims 1-33 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Patent Agent and Attorney for Applicants

By: 
Richard F. Frankeny
Reg. No. 47,573
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
Dallas, Texas 75201
(512) 370-2872